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SOpenCL: An Infrastructure for Transparently Integrating FPGAs in Heterogeneous, Accelerator-Based Systems[1]

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Abstract

The use of heterogeneous parallel architectures appears as a promising approach in the HPC domain, due to both the absolute performance and the high performance/power ratio these architectures offer. Heterogeneous systems are typically organized as a number of computational accelerators, such as GPUs, DSPs etc., complementing one or more general purpose CPUs. Field Programmable Gate Arrays (FPGAs) are hardware devices that offer a sea of gates and memory islands which can be configured as digital circuits, thus implementing algorithms at the hardware level. FPGAs are an excellent accelerator choice, as they can often prove more power-efficient than conventional CPUs and even GPUs.

Despite the favorable power/performance characteristics, the adoption of FPGAs in the HPC domain is rather limited. The implementation of algorithms at the hardware-level requires experience on hardware design and the use of specialized hardware-description languages (Verilog, VHDL, SystemC), thus remaining outside the realm of domain experts and software engineers. In this talk we present SOpenCL, a tool infrastructure that facilitates the wider use of FPGAs in reconfigurable systems. SOpenCL translates algorithmic descriptions at the software level to equivalent circuit descriptions in Verilog, which can then be directly implemented on an FPGA. We use OpenCL, a popular and industry supported parallel programming standard for heterogeneous systems, as the programming model of choice for the software-level algorithmic descriptions. This way, programs targeted at CPUs or GPUs can transparently and without any further development effort be executed on FPGA-based accelerator systems as well.

Key words: Heterogeneous Systems, OpenCL, FPGAs, High-level synthesis.

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